WHAT IS CLAIMED IS:

1. A system for correcting duty-cycle distortion, comprising:

a measurement unit to measure duty-cycle distortion in a clock signal; and

a correction unit to dynamically adjust the clock signal to reduce the duty-cycle distortion.

2. The system of claim 1, wherein the correction unit adjusts durations of high- phase and low-phase portions of the clock signal to reduce the duty-cycle distortion to substantially zero.

3. The system of claim 1, wherein the measurement unit includes:

a single-input charge pump driven by the clock signal; and

a loop filter to integrate an output of the charge pump to form an analog correction signal for the correction unit.

4. The system of claim 3, wherein the measurement unit computes an average of the output current of the charge pump over a predetermined time, said average output current being proportional to the duty-cycle distortion.

5. The system of claim 1, wherein the measurement unit generates an analog control signal to adjust a duty cycle of the clock signal.

6. The system of claim 5, wherein the analog control signal adjusts the duty cycle of the clock signal by an amount which corrects substantially all the duty-cycle distortion.

7. The system of claim 5, wherein the correction unit includes:

a delay unit to delay an input signal based on the analog control signal, said delayed input signal corresponding to the frequency signal having reduced duty-cycle distortion.

8. The system of claim 5, wherein the measurement unit includes a signal generator which generates the analog control signal, said signal generator including:

a control unit;

a positive current source; and

a negative current source,

wherein the control unit selectively connects the positive current source and the negative current source to an output node of the signal generator to generate the analog control signal.

9. The system of claim 8, wherein the control unit connects the positive current source and the negative current source to the output node for different periods of time to generate the analog control signal.

10. A duty-cycle correction circuit, comprising:

a voltage-controlled buffer to generate an output clock signal based on an input clock signal and a control voltage;

a single-input charge pump to receive a core clock signal and a bias voltage; and

a bias generator to generate said control voltage based on an output of the single-input charge pump and to feedback said control voltage to the single-input charge pump.

11. The circuit of claim 10, wherein the voltage-controlled buffer corrects the input clock signal to have reduced phase distortion.

12. The circuit of claim 10, further comprising:

a startup circuit to generate an initial DC bias voltage for the single-input CP; and

a loop filter to provide a correction voltage to the bias generator.

13. The circuit of claim 12, wherein the loop filter converts an output current of the single-input charge pump to the correction voltage.

14. The circuit of claim 10, wherein the bias generator compensates for changes in a supply voltage.

15. The circuit of claim 11, wherein a response time is approximately 50 nS.

16. The circuit of claim 10, further comprising:

a global clock network to distribute the output clock signal.

17. The circuit of claim 10, wherein the single-input charge pump measures duty- cycle distortion of the core clock signal and generates an average current signal proportional to the duty cycle distortion of the core clock signal.

18. The circuit of claim 17, wherein the current signal is converted to a correction voltage, and wherein the correction voltage determines a value of the control voltage.

19. A method for correcting duty-cycle distortion, comprising:

measuring duty-cycle distortion in a clock signal; and

dynamically adjusting the clock signal to reduce the duty-cycle distortion.

20. The method of claim 19, wherein measuring the duty-cycle distortion includes:

measuring durations of high-phase and low-phase portions of the clock signal.

21. The method of claim 20, further comprising:

generating an analog control signal based on said durations,

wherein the clock signal is adjusted to cause the duration of the high-phase portion of the clock signal to equal the low-phase portion of the clock signal.

22. The method of claim 21, wherein the analog control signal adjusts the duty cycle of the frequency signal by an amount which corrects substantially all the duty-cycle distortion.

23. The method of claim 22, further comprising:

delaying an input signal based on the analog control signal, said delayed input signal corresponding to the frequency signal having reduced duty-cycle distortion.

24. A processing system, comprising:

a circuit; and

a correction unit to correct duty cycle distortion of a frequency signal input into the circuit, said correction unit comprising a measurement unit to measure duty-cycle distortion in a clock signal and a correction unit to dynamically adjust the clock signal to reduce the duty-cycle distortion.

25. The processing system of claim 24, wherein said circuit includes a chipset, processor, or memory.